IN THE CLAIMS

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9. (Currently amended) A buffer management system for controlling access of a first buffer operation and a second buffer operation to a shared buffer to prevent overwriting of data not yet read or reading of locations to which valid data has not yet been written, comprising

a buffer manager that is configured to assert a wrap signal when the first buffer operation involves consecutively accessing each buffer location of a block of buffer locations assigned sequential address values in an order different than an order defined by the sequential address values, and is further configured to limit accesses to the buffer of the second buffer operation in dependence upon the wrap signal.

10. (Previously presented) The buffer management system of claim 9, wherein

the first buffer operation includes an access that is based on a block address and an offset address, and

the second buffer operation is limited to the block address when the wrap signal is asserted, and is limited to a combination of the block address and the offset address when the wrap signal is deasserted.

11. (Previously presented) The buffer management system of claim 10, wherein

a change of limit of the second access is communicated via a gray-code sequence.

12. (Previously presented) The buffer management system of claim 10, wherein

the buffer manager is further configured to assert an idle signal when the first buffer operation terminates, and

the second buffer operation is further limited to the block address when the idle signal is asserted.

13. (Previously presented) The buffer management system of claim 9, wherein

the first access and the second buffer operations correspond to:

a series of write-accesses to the buffer, and

a series of read-accesses to the buffer.

14. (Currently amended) A method of controlling access of a first buffer operation and a second buffer operation to a shared buffer to prevent overwriting of data not yet read or reading of locations to which valid data has not yet been written ~~to a buffer~~ comprising:

determining a block address and an offset address corresponding to the~~a~~ first buffer operation involving consecutively accessing each buffer location of a block of buffer locations assigned sequential block address values,

determining when the offset address is non-sequential relative to the block address wherein the buffer locations are accessed in an order different than an order defined by the sequential address values, and

limiting access of the~~a~~ second buffer operation to locations within the block when the offset address is non-sequential.

15. (Previously presented) The method of claim 14, further including:

determining when the offset address is sequential relative to the block address, and

limiting accesses of the second buffer operation to a combination of the block address and the offset address when the offset address is sequential.

16. (Previously presented) The method of claim 14, wherein

limiting the accesses of the second buffer operation includes determining a gray-code sequence corresponding to a change in the block address.